

CLAIMS

What is claimed is:

1. An integrated circuit active memory device comprising:

a command engine operable to generate either respective sequences of array control unit commands or respective sequences of memory device control unit commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the array control unit commands from the command engine, the array control unit being operable to generate a respective sequence of processing element instructions responsive to each of the array control unit commands;

a memory device control unit coupled to receive the memory device control unit commands from the command engine, the memory device control unit being operable to generate a respective sequence of memory commands responsive to each of the memory device control unit commands;

a decode memory device coupled to receive the processing element instructions from the array control unit, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions;

a memory device having a data bus containing a plurality of data bus bits, the memory device being operable to receive the memory commands and couple write data to and read data from the memory device through the data bus; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the processing element microinstructions from the decode memory for controlling the operation of the processing elements.

2. The active memory device of claim 1 wherein the memory device comprises a random access memory device.

3. The active memory device of claim 2, wherein the decode memory device comprises a static random access memory device.

4. The active memory device of claim 1, further comprising:  
a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

5. The active memory device of claim 1 wherein the array control unit is further operable to generate an array control unit instruction along with each of the processing element instructions, the array control unit instruction controlling the operation of the array control unit.

6. The active memory device of claim 1 wherein the array control unit further comprises:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and one of the processing element instructions, the array control unit microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored.

7. The active memory device of claim 6, further comprising a program port coupled to the program cache device, the program port receiving the array control unit instructions, and coupling the array control unit instructions to the program cache device to program the program cache device prior to operation of the array control unit.

8. The active memory device of claim 1, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

9. An integrated circuit active memory device comprising:

a command engine operable to generate either respective sequences of array control unit commands or respective sequences of memory device control unit

commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the array control unit commands from the command engine, the array control unit comprising:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and a processing element instruction, the array control unit microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored;

a memory device control unit coupled to receive the memory device control unit commands from the command engine, the memory device control unit being operable to generate a respective sequence of memory commands responsive to each of the memory device control unit commands;

a decode memory device coupled to receive the processing element instructions from the program cache, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions;

a memory device having a data bus containing a plurality of data bus bits, the memory device being operable to receive the memory commands and couple write data to and read data from the memory device through the data bus; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the processing element microinstructions from the decode memory for controlling the operation of the processing elements.

10. The active memory device of claim 9, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

11. The active memory device of claim 9, further comprising a program port coupled to the program cache device, the program port receiving the processing element instructions and coupling the processing element instruction to the program cache device to program the program cache device prior to operation of the array control unit.

12. The active memory device of claim 9, further comprising a program port coupled to the program cache device and to the decode memory device, the program port receiving the processing element instructions and coupling the processing element instruction to the program cache device for storage in the program cache device prior to operation of the array control unit, the program port further receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device for storage in the decode memory device prior to operation of the array control unit, the processing element microinstructions stored in the decode memory corresponding to the processing element instructions stored in the program cache device.

13. The active memory device of claim 9 wherein the decode memory device comprises a random access memory device.

14. The active memory device of claim 13 wherein the decode memory device comprises a static random access memory device.

15. The active memory device of claim 9, further comprising:  
a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store at least a portion of each of a plurality of the processing element instructions and to simultaneously output the stored portions of the processing element instructions as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

16. An integrated circuit single instruction multiple data processing device, comprising:

a command engine operable to generate respective sequences of array control unit commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the array control unit commands from the command engine, the array control unit comprising:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and a processing element instruction, the

array control unit microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored;

a decode memory device coupled to receive the processing element instructions from the program cache, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the processing element microinstructions from the decode memory for controlling the operation of the processing elements.

17. The processing device of claim 16, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

18. The processing device of claim 16, further comprising a program port coupled to the program cache device, the program port receiving the processing

element instructions and coupling the processing element instruction to the program cache device to program the program cache device prior to operation of the array control unit.

19. The processing device of claim 16, further comprising a program port coupled to the program cache device and to the decode memory device, the program port receiving the processing element instructions and coupling the processing element instruction to the program cache device for storage in the program cache device prior to operation of the array control unit, the program port further receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device for storage in the decode memory device prior to operation of the array control unit, the processing element microinstructions stored in the decode memory corresponding to the processing element instructions stored in the program cache device.

20. The processing device of claim 16 wherein the decode memory device comprises a random access memory device.

21. The processing device of claim 20 wherein the decode memory device comprises a static random access memory device.

22. The processing device of claim 16, further comprising:  
a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store at least a portion of each of a plurality of the processing element instructions and to simultaneously output the stored portions of the processing element instructions as a processing element microinstruction; and



a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

23. An active memory control system, comprising:

a first control device receiving task commands corresponding to respective active memory operations, the first control device being operable to generate either a respective set of memory commands or a respective set of processing commands responsive to each of the task commands;

a second control device coupled to receive the memory commands from the first control device, the second control device being operable to generate a respective set of the memory device instructions responsive to each of the memory commands;

a third control device coupled to receive the processing commands from the first control device, the third control device being operable to generate a respective set of the processing element instructions responsive to each of the processing commands.

a decode memory device coupled to receive the processing element instructions from the third control device, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions.

24. The active memory control system of claim 23, wherein the decode memory device comprises a random access memory device.

25. The active memory control system of claim 24, wherein the decode memory device comprises a static random access memory device.

26. The active memory control system of claim 23, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the third control device, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, the multiplexer being operable to couple either the first input or the second input to an output.

27. The active memory control system of claim 23 wherein the third control device is further operable to generate a control instruction along with each of the processing element instructions, the control instruction controlling the operation of the third control device.

28. The active memory control system of claim 23 wherein the third control device further comprises:

a program cache device containing a plurality of instructions, at least some of the instructions including a control unit microinstruction and one of the processing element instructions, the control unit microinstructions being passed to the third control device to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the third control device, at least some of the control signals being responsive to the control unit microinstruction to cause the cache control device to access a specific location in the cache control device where one of the instructions is stored.

29. The active memory control system of claim 28, further comprising a program port coupled to the program cache device, the program port receiving the instructions, and coupling the instructions to the program cache device to program the program cache device prior to operation of the third control device.

30. A computer system, comprising:

a host processor having a processor bus;

at least one input device coupled to the host processor through the processor bus;

at least one output device coupled to the host processor through the processor bus;

at least data storage device coupled to the host processor through the processor bus; and

an active memory device, comprising:

a command engine operable to generate either respective sequences of array control unit commands or respective sequences of memory device control unit commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the array control unit commands from the command engine, the array control unit being operable to generate a respective sequence of processing element instructions responsive to each of the array control unit commands;

a memory device control unit coupled to receive the memory device control unit commands from the command engine, the memory device control unit being operable to generate a respective sequence of memory commands responsive to each of the memory device control unit commands;

a decode memory device coupled to receive the processing element instructions from the array control unit, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions;

a memory device having a data bus containing a plurality of data bus bits, the memory device being operable to receive the memory commands and couple write data to and read data from the memory device through the data bus; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the processing element microinstructions from the decode memory for controlling the operation of the processing elements.

31. The computer system of claim 30 wherein the memory device comprises a random access memory device.

32. The computer system of claim 31, wherein the decode memory device comprises a static random access memory device.

33. The computer system of claim 30, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

34. The computer system of claim 30 wherein the array control unit is further operable to generate an array control unit instruction along with each of the processing element instructions, the array control unit instruction controlling the operation of the array control unit.

35. The computer system of claim 30 wherein the array control unit further comprises:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and one of the processing element instructions, the array control unit microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored.

36. The computer system of claim 35, further comprising a program port coupled to the program cache device, the program port receiving the array control unit instructions, and coupling the array control unit instructions to the program cache device to program the program cache device prior to operation of the array control unit.

37. The computer system of claim 30, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

38. A computer system, comprising:  
a host processor having a processor bus;  
at least one input device coupled to the host processor through the processor bus;  
at least one output device coupled to the host processor through the processor bus;  
at least data storage device coupled to the host processor through the processor bus; and  
an active memory device, comprising:  
a first control device receiving task commands from the host processor corresponding to respective active memory operations, the first control device being

operable to generate either a respective set of memory commands or a respective set of processing commands responsive to each of the task commands;

a second control device coupled to receive the memory commands from the first control device, the second control device being operable to generate a respective set of the memory device instructions responsive to each of the memory commands;

a third control device coupled to receive the processing commands from the first control device, the third control device being operable to generate a respective set of the processing element instructions responsive to each of the processing commands.

a decode memory device coupled to receive the processing element instructions from the third control device, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions.

a memory device having a data bus containing a plurality of data bus bits, the memory device being coupled to second control device to receive the memory device instructions and couple write data to and read data from the memory device through the data bus responsive to the memory device instructions; and

an array of processing elements each of which is coupled a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to the third control device to receive the processing element microinstructions for controlling the operation of the processing elements.

39. The computer system of claim 38, wherein the decode memory device comprises a random access memory device.

40. The computer system device of claim 39, wherein the decode memory device comprises a static random access memory device.

41. The computer system device of claim 38, further comprising:  
a plurality of instruction registers coupled to receive the processing element instructions from the third control device, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, the multiplexer being operable to couple either the first input or the second input to an output.

42. The computer system of claim 38 wherein the third control device is further operable to generate a control instruction along with each of the processing element instructions, the control instruction controlling the operation of the third control device.

43. The computer system of claim 38 wherein the third control device further comprises:

a program cache device containing a plurality of instructions, at least some of the instructions including a control unit microinstruction and one of the



processing element instructions, the control unit microinstructions being passed to the third control device to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the third control device, at least some of the control signals being responsive to the control unit microinstruction to cause the cache control device to access a specific location in the cache control device where one of the instructions is stored.

44. The computer system of claim 43, further comprising a program port coupled to the program cache device, the program port receiving the instructions, and coupling the instructions to the program cache device to program the program cache device prior to operation of the third control device.

45. A method of controlling the operation of a memory device and an array of processing elements that are coupled to the memory device, the method comprising:

receiving a task command corresponding to an active memory operation;  
generating either a set of array commands or a set of memory device commands responsive to the task command;

generating a respective set of processing element instructions responsive to each of the array commands;

generating a respective set of memory device instructions responsive to each of the memory device commands;

selecting a processing element microinstruction responsive to each of the processing element instructions, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the corresponding processing element instructions;

controlling the memory device responsive to the memory device instructions; and

controlling the processing elements in the array responsive to the processing element microinstructions.

46. The method of claim 45 wherein at least some of the processing element instructions comprise respective storage device addresses, and wherein the act of selecting a processing element microinstruction comprises:

storing the processing element microinstructions at respective addresses in a storage device; and

using the processing element instructions to address the storage device.

47. The method of claim 46 wherein the act of storing the processing element microinstructions comprises storing the processing element microinstructions in the storage device prior to operation of the a memory device and processing elements based on the operations that are to be performed by the memory device or processing elements.

48. The method of claim 46, further comprising combining at least portions of a plurality of the processing element instructions and simultaneously outputting the combined processing element instructions as an extra length one of the processing element microinstructions.

49. A method of processing data, comprising:

receiving a task command corresponding to a processing operation;

generating a set of processing commands responsive to the task command;

generating a respective set of processing element instructions responsive to each of the processing commands;

selecting a processing element microinstruction responsive to each of the processing element instructions, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the corresponding processing element instructions; and

processing the data responsive to the processing element microinstructions.

50. The method of claim 49 wherein at least some of the processing element instructions comprise respective storage device addresses, and wherein the act of selecting a processing element microinstruction comprises:

storing the processing element microinstructions at respective addresses in a storage device; and

using the processing element instructions to address the storage device.

51. The method of claim 49 wherein the act of storing the processing element microinstructions comprises storing the processing element microinstructions in the storage device prior to operation of the processing elements based on the operations that are to be performed by the processing elements.

52. The method of claim 49, further comprising combining at least portions of a plurality of the processing element instructions and simultaneously outputting the combined processing element instructions as an extra length one of the processing element microinstructions.